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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,892	07/09/2003	Cheng-Ming Yih	4425-306	8433

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EXAMINER	
TRAN, MAI HUONG C	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,892	YIH ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,248,641 to Liu et al. (hereinafter Liu) in view of Doong et al. (6,429,081) (hereinafter Doong).

Regarding to claims 1, 2 and 7, Liu discloses a semiconductor device comprising a substrate 11; at least a trench isolation device that comprises a first portion on the substrate and a second portion in the substrate (fig. 2G); a spacer 23a at a sidewall of the first portion, wherein the spacer covers a corner between the sidewall and the substrate 11 as set forth in col. 2, lines 40-67, col. 3, lines 1-14, and figures 2D, 2G.

However, Liu does not disclose at least a nonvolatile memory using trench isolation device. Doong teaches a flash memory which is a nonvolatile memory using trench isolation device (col. 4, lines 53-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the trench isolation device of Liu into the nonvolatile memory as taught by Doong in order to have high reliability of the flash memories (col. 1, lines 23-24) and to improve programming speed and data retention (col. 4, lines 18-19).

Regarding to claims 3, 11, and 16, Liu discloses the structure wherein the spacer is deposited silicon dioxide (col. 2, lines 62-67, col. 3, line 1, and col. 3, line 18).

Regarding to claims 4, 12, and 17, Liu discloses the claimed invention except for the structure wherein the spacer is deposited silicon nitride or other isolated materials. However, Doong discloses the structure wherein the spacer is deposited silicon nitride (col. 8, lines 44-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure wherein the spacer is deposited silicon nitride, as taught by Doong in order to have high reliability (col. 1, lines 23-24) and to improve programming speed and data retention (col. 4, lines 18-19).

Regarding to claims 5, 10, and 15, Liu discloses the structure wherein a formation of the spacer comprises following steps of depositing a dielectric material layer 17 onto the substrate 11 and the trench isolation device 12; and etching the dielectric material

layer to form the spacer 23a at the sidewall of the first portion (col. 3, lines 5-20, and fig. 2G).

Regarding to claims 6 and 8, Liu discloses the structure wherein the trench isolation device is shallow trench isolation (col. 3, lines 13, and fig. 2G).

Regarding to claim 9, Liu discloses the claimed invention except for the nonvolatile memory is flash memory. Doong discloses the nonvolatile memory is flash memory (col. 6, line 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the nonvolatile memory that is a flash memory, as taught by Doong in order to have high reliability of the flash memories (col. 1, lines 23-24) and to improve programming speed and data retention (col. 4, lines 18-19).

Regarding to claim 13, Liu discloses the claimed invention except for the nonvolatile memory comprises a tunnel oxide layer. Doong teaches the nonvolatile memory comprises a tunnel oxide layer 412 (col. 9, lines 32-35, and fig. 14b).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the nonvolatile memory that comprises a tunnel oxide layer, as taught by Doong in order to have high reliability of the flash memories (col. 1, lines 23-24) and to improve programming speed and data retention (col. 4, lines 18-19).

Regarding to claim 14, Liu discloses a semiconductor device comprising a substrate 11; a shallow trench isolation comprises a first portion on the substrate and a second portion in the substrate (fig. 2G); a spacer 23a at a sidewall of the first portion of the shallow trench isolation, wherein the spacer covers a corner between the sidewall and the substrate 11 as set forth in col. 2, lines 40-67, col. 3, lines 1-14, and figures 2D, 2G.

However, Liu does not disclose at least a flash memory between two shallow trench isolations. Doong teaches a flash memory between two shallow trench isolations (col. 4, lines 53-67 and fig. 21b).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a flash memory between two shallow trench isolations, as taught by Doong in order to have high reliability of the flash memories (col. 1, lines 23-24) and to improve programming speed and data retention (col. 4, lines 18-19).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mht
9/2/04

Mai-Huong Tran
Examiner
Art Unit 2818